REMARKS

Claims 1-19 are pending in the present application. Claims 20-43 were previously cancelled. No new matter has been added.

Claims 1, 2, 4, 5, 9, 11, and 12-16 have been rejected under 35 U.S.C. § 102(e) as assertedly being anticipated by U.S. Patent Application Publication No. 2003/0011032 A1 to Umebayashi (hereinafter "Umebayashi"). Claim 3 has been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 2 above, and further in view of U.S. Patent No. 6,686,248 B1 to Yu (hereinafter "Yu"). Claims 6, 7, 17, and 18 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 1 above, and further in view of U.S. Patent No. 6,873,051 B1 to Paton et al. (hereinafter "Paton"). Claims 8 and 19 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 1 above, and further in view of U.S. Patent No. 6,797,641 B2 to Holmes et al. (hereinafter "Holmes"). Claim 10 has been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 1 above, and further in view of U.S. Patent No. 5,994,759 to Darmawan et al. (hereinafter "Darmawan"). Applicants respectfully traverse these rejections.

The Office Action asserted that Umebayashi discloses a *dummy silicide structure* as recited in Applicants' claims 1 and 13, referring to "the dummy silicided gate 71, the right gate of the plurality of gates numbered 71 in the figure [5A]" of Umebayashi. (Office Action, page 2.) In Applicants' previous response dated August 3, 2005, Applicants pointed out that a "dummy silicide structure" within the context of

Applicants' patent application "does not perform a logical function for the circuitry contained on the semiconductor chip." (Applicants' patent application, paragraph 32.)

Applicants further pointed out that structures numbered 71 of Umebayashi refer to a gate and a word line that are formed in trenches. Generally, the process disclosed in Umebayashi involves forming dummy gate patterns 71 as described in paragraph 62 with reference to Figures 4A-4B. The dummy gate patterns 71 are used as masks to form the low concentration diffusion layers 72 (*e.g.*, the source/drain regions). (Umebayashi, paragraph 63.) An insulating film 18 is deposited over the dummy gate patterns 71 (Umebayashi, paragraph 68, Figures 5A-5B), and a CMP process is performed to expose the top of the dummy gate patterns 71 (Umebayashi, paragraph 71, Figures 6A-6B). Thereafter, the material of the dummy gate patterns 71 is replaced. (Umebayashi, paragraph 72-74, Figures 7A-7B.)

Neither of the dummy gate patterns 71, however, are a "dummy silicide structure" as recited by Applicants' claim 1 and 13. In fact, the dummy gate pattern 71 on the right-hand side of Figure 5A of Umebayashi, which was referred to by the Office Action (see Office Action, pages 2-3), is ***a word line***, *not a dummy structure as recited by Applicants' claims 1 and 13.* Umebayashi states that, in reference to Figure 1, "[t]he trench 81 formed in the first interlayer insulating film 18 is disposed on the element separating region 12 of the logic region, and a *word line* 84 is formed within the trench 81." (Umebayashi, paragraph 39.) (Emphasis added.) The word line 84 of Figure 1 corresponds to the dummy gate pattern 71 on the right-hand side of Figure 5A. Thus, *the dummy gate pattern 71 of Umebayashi is not a dummy structure as recited in Applicants' claims 1 and 13.*

This is further explained in paragraph 13 of Umebayashi.

> Further, according to the present invention, there is provided a semiconductor device, whrerein an element separating region is formed on the semiconductor substrate, and a word line connected to the gate electrode is formed so as to be connected to the gate electrode provided in the trench which is formed on the semiconductor substrate and the element separating region.

(Umebayashi, paragraph 13.)

In response to Applicants' arguments, the Office Action stated:

> Applicants argue that the dummy gate of the [Umebayashi] reference . . . is not a dummy gate . . . However, [Umebayashi] discloses in figure 5A, that the gate has separating trench isolation right beneath it. Therefore, it does not function as a conventional gate, hence it is a dummy, or non-functional gate. Even though, the gate is connected to connection 41, it does not play a role in device operation. Note that it is surrounded on all sides (except the top) by insulators 21 and 76 (of figures 5A) and 12 (of figure 3A), and it does not in any way acts (*sic*) as an active circuit element such as an active gate, which includes corresponding source and drain regions would (*sic*).

(Office Action, pages 5-6.)

This is simply irrelevant and incorrect. While the right-most structure 71 in figure 5A of Umebayashi is formed over an isolation trench, it is not a gate, and as such does not require source/drain regions. Rather, the right-most structure 71 in figure 5A of Umebayashi is a *word line* as discussed above, and as such, may be formed on an isolation trench.

Therefore, figure 5A of Umebayashi fails to disclose a dummy structure as recited in Applicants' claims. Because the cited reference, Umebayashi, does not disclose a "dummy silicide structure" as recited in Applicants' claims 1 and 13, it is respectfully requested that the rejections of claims 1 and 13 under 35 U.S.C. § 102(e) be withdrawn. Claims 2-12 and 14-19 depend from and further limit independent claims 1 and 13, and

accordingly, it is also respectfully requested that the rejections of dependent claims 2-12 and 14-19 be withdrawn as well.

In view of the above, Applicants respectfully submit that this response complies with 37 C.F.R. § 1.116. Applicants further submit that the claims are in condition for allowance. No new matter has been added by this amendment. If the Examiner should have any questions, please contact Applicants' attorney at the number listed below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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